Fully Depleted Pinned Photodiode CMOS Image Sensor With Reverse Substrate Bias

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Konstantin D. Stefanov, *Member, IEEE,* Andrew S. Clarke and Andrew D. Holland

***Abstract*—A new pixel design using fully depleted pinned photodiode (PPD) in a 180 nm CMOS image sensor (CIS) process has been developed and the first experimental results from a test chip are presented. The sensor can be fully depleted by means of reverse bias applied to the substrate, and the principle of operation is applicable to very thick sensitive volumes. Additional n-type implants under the in-pixel p-wells have been added to the manufacturing process in order to eliminate the large parasitic substrate current that would otherwise be present in a normal device. The new design shows the same electro-optical performance as the PPD pixel it is based on, and can be fully depleted without significant leakage currents. This development has the potential to greatly increase the quantum efficiency of scientific PPD CIS at near-infrared and soft X-ray wavelengths.**

***Index Terms*—CMOS image sensor (CIS), pinned photodiode (PPD), full depletion, reverse bias.**

I. Introduction

CMOS image sensors (CIS) based on the pinned photodiode (PPD) [1] are widely used today in high performance imaging. For scientific imaging, for example in astronomy and X-ray detection, hybrid CIS and backside-illuminated (BSI) charge coupled devices (CCD) are routinely made on high resistivity bulk silicon, and can achieve full depletion over the entire device thickness, in excess of 200 µm. This greatly increases the quantum efficiency (QE) in the near-infrared (IR) and soft X-ray (<10 keV) regions, and is highly desirable in many other applications.

Although hybrid CIS with high QE are successfully manufactured and used, a monolithic PPD-based CIS with the same high QE would be very attractive. Due to the small sense node and the local charge-to-voltage conversion, monolithic PPD CIS can achieve sub-electron read noise [2]-[3], something that is beyond the reach of hybrid or non-PPD CIS. In addition, monolithic imagers are usually simpler to manufacture, have better yield and are less expensive.

Thick sensitive semiconductor volumes are depleted by applying reverse bias across the substrate, so that field-free regions are eliminated and the photogenerated charge is promptly collected at the photodiodes (in the case of CIS) [4]-[5], or in the buried channel of CCDs [6]. The red and near-IR QE increases with the thickness of the sensor [4], however due to the lateral charge diffusion during the increased transit time the spatial resolution deteriorates [6]. The magnitude of the reverse bias depends on the resistivity and the thickness of the semiconductor substrate and can far exceed any other voltage in the system. The structures of both hybrid CIS and CCDs appear as reverse biased pn junctions, and this allows operation without undesirable leakage currents.

PPD CIS are active pixel sensors which contain at least 3 transistors in a p-well next to the PPD. Individual pixels are separated by shallow trench insulation (STI) placed in a p-well, which is a continuation of the transistor p-well. The front side p-wells are at the sensor's substrate potential and are externally connected to ground. Applying negative substrate bias V_{BSB} at the back of the device in order to increase the depletion depth under the PPD would result in large currents flowing from the front side p-wells to the backside p^{++} contact, as the $p^{+}/p^{-}/p^{++}$ structure conducts resistively. Eliminating this parasitic current would allow the full substrate thickness to be depleted, and is the main objective of this development.

II. Design and Operation

The new pixel design implements a deep, lightly doped n-type implant under the in-pixel p-wells, as shown in Fig. 1. This implant, called "deep depletion extension" (DDE) is floating and does not connect to the PPDs.

In normal operation the DDE acquires its potential from the adjacent PPDs and becomes depleted, as described in detail in [7]. By choosing the appropriate doping profile and size of the DDE, its potential can be made lower than the pinning voltage V_{pin}, but still high enough to create a potential barrier. The DDE region acts as a bridge extending the depletions from the PPDs underneath the p-wells, creating a pinch-off and a potential barrier of sufficient height to prevent thermionic emission of holes from the p-wells towards the substrate.

Fig. 2(a) and Fig. 2(b) show the potential distribution in a simplified 3-pixel simulation model without and with the DDE implant, respectively, using the same PPD under reverse bias. The difference in the potential barrier in depth under the p-wells can be clearly seen, and in the case of medium depth DDE implant is around 0.7 V.

Along the line of charge transfer the DDE region can have very low lateral electric field, which could slow down charge collection. If the DDE is too wide or highly doped, a potential

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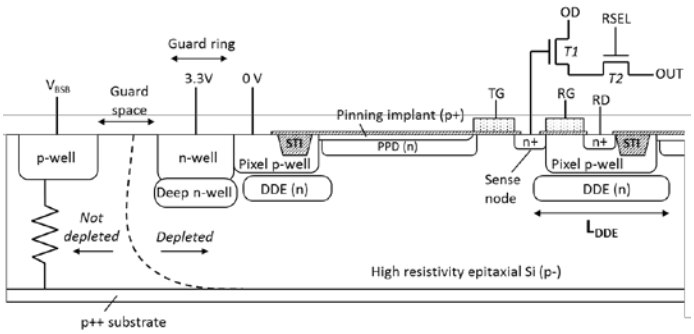

Fig. 1. Cross section of the proposed 4T PPD pixel design along the central line of charge transfer and the reverse biasing structure. The two readout transistors T1 and T2 are physically situated in the p-well, and the reset transistor is formed between the reset drain (RD) and the sense node.

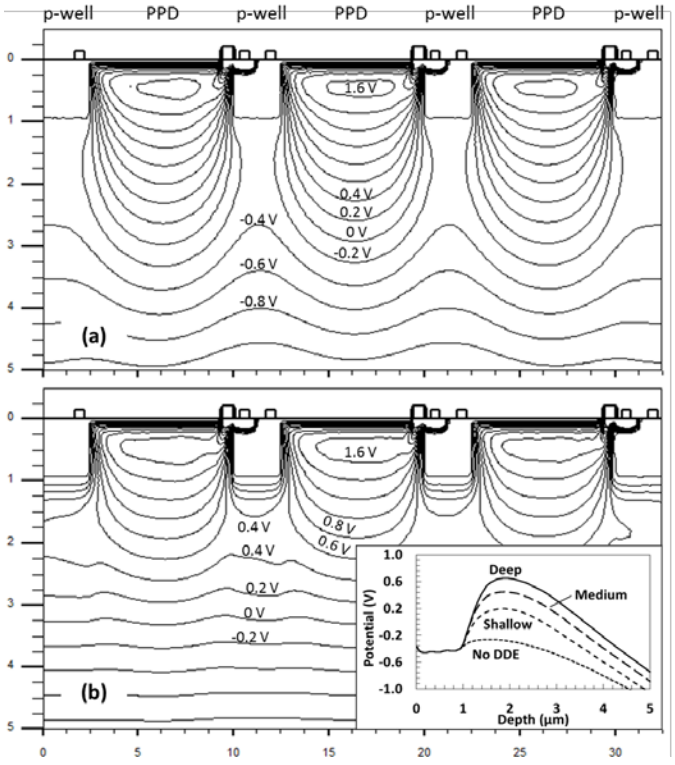

Fig. 2. Potential diagrams in a simplified 3-pixel, 10 µm pitch PPD model with V_{pin} =1.7V under reset conditions. The simulation is for 18 µm, 1000 Ω.cm epitaxial silicon, reverse biased at -5V: (a) normal pixel without DDE; (b) DDE pixel with medium implant depth. The equipotential lines are spaced 0.2V apart, and the dimensions are in microns. The inset shows the potential in depth through a p-well for (a) and for three different DDE profiles.

pocket could be formed in its place, or it may not deplete at all. To prevent this, the size of the p-well was reduced to the minimum width allowed under the design rules for the process, around 2 µm. This helps achieve the desired potentials, but is not sufficient. Significant work was done to optimize the shape, size and dopant profile of the DDE implant using 2D and 3D TCAD tools, taking into account a number of constraints from the manufacturing process. This was crucial to achieve the desired operation while minimizing the disturbance to the potentials of the PPD.

To test this concept, a chip containing pixel arrays on 10 µm and 5.4 µm pitch was designed at the CEI and manufactured by TowerJazz Semiconductor using their well-established 180 nm image sensor process on 18 µm thick, 1000 Ω.cm epitaxial wafers. The chip contains 4 pixel design variants of each pitch, with DDE implants with length L_{DDE} overlapping the in-pixel p-well in increasing steps. Three process variants with different depth of the DDE were manufactured – shallow, medium and deep, in addition to producing a reference design where the only difference was that the DDE implant was omitted.

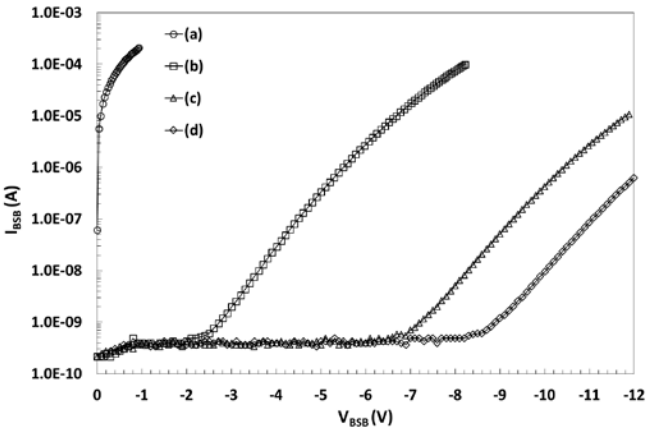

Fig. 3. Whole chip reverse currents in darkness at 23±1 °C, V_{pin}=1.7V: (a) reference design (no DDE); (b) shallow DDE profile; (c) medium DDE profile; (d) deep DDE profile. The chip size is 5 mm × 5 mm.

III. Experimental Results

A. Leakage Current and Photo Response

Fig. 3 shows the measured reverse substrate current for the reference device and for 3 device variants with different implantation profiles. The current is measured in the substrate connection and is the sum of the leakage currents from the individual pixel arrays. It is dominated by the least-performing design, and includes the contribution from other structures, such as the row addressing logic, output buffers and ESD protection circuitry. The leakage current clearly depends on the DDE doping profile, which is an indication that it occurs in the pixel arrays and not elsewhere on chip.

The onset of higher leakage current is caused by thermionic emission [8] of holes over the potential barrier in the DDE region. The barrier height is reduced almost linearly by the applied reverse voltage, similar to the way the potential in the buried channel in CCDs is manipulated by the applied gate voltage [9]. This leakage mechanism has exponential dependence on the applied reverse voltage, as the data in Fig. 3 shows, and is triggered above a threshold dependent on device structure and doping profiles. The threshold voltage increases with the barrier height created by the DDE, shown in the inset of Fig.2 for V_{BSB} = -5V. This leakage, however, is not a serious limitation; provided that the threshold is above the voltage required to achieve full depletion, the device achieves its objectives.

Most of the new pixel variants exhibit nearly identical electro-optical performance to the reference, as shown from the photon transfer curves (PTC) [10] in Fig. 4. The measured conversion gain for the 10 µm and 5.4 µm pixels was 78 µV/e- and 38 µV/e-, close to the design values.

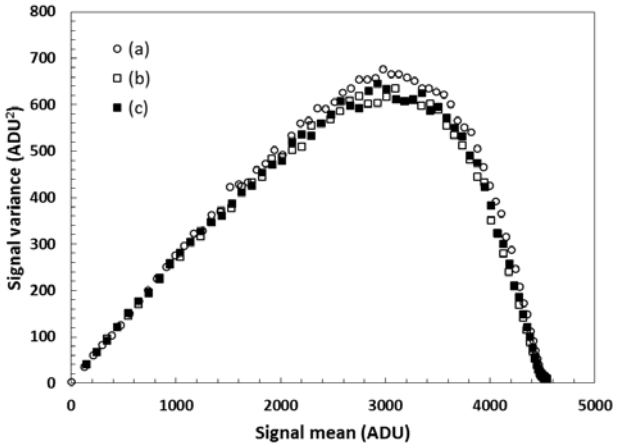

Fig. 4. Photon transfer curve of a 10 µm pixel: (a) reference (no DDE); (b) medium DDE doping with substrate bias of 0V; and (c) medium DDE with substrate bias of -5V. One ADU is 305µV.

As PPDs accumulate photogenerated or dark current charge, their peak potential is reduced and becomes lower than V_{pin}. This lowers the potential barrier under the p-wells because it is determined by the adjacent PPDs, and in turn can increase the reverse current. However, due to the large PPD storage capacitance this potential reduction is relatively small, and as shown in Fig. 5, illumination far beyond full well capacity does not result in undesired sudden reverse current increase.

B. Depletion Depth

The device was designed to be backside illuminated with the reverse bias supplied from the front, using the undepleted area at the chip periphery as shown in Fig. 1. This area is approximately 600 µm wide (for a chip with size 5 mm × 5 mm), and provides a conductive path to the backside with measured front-to-back resistance of 21 Ω. All off-pixel circuitry is situated above a deep n-well, biased to 3.3V. In the case of BSI processed device, the substrate is removed and the backside is p^{++} implanted with a shallow dopant.

For the selected epitaxial material and V_{pin} the simulated V_{BSB} for full depletion was estimated at around -4V (using the model in Fig. 2), which implies that every pixel variant in chips with medium and deep DDE profiles can be fully depleted. Dark current measurements were used to estimate

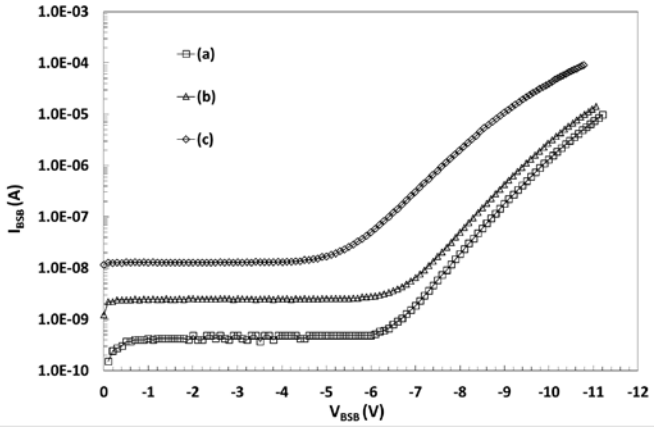

Fig. 5. Whole chip reverse currents at 23±1 °C, V_{pin}=1.7V, medium DDE: (a) in darkness, (b) light signal near full well capacity (3,000 ADU, 12 ke-); (c) light signal at 10 times full well capacity.

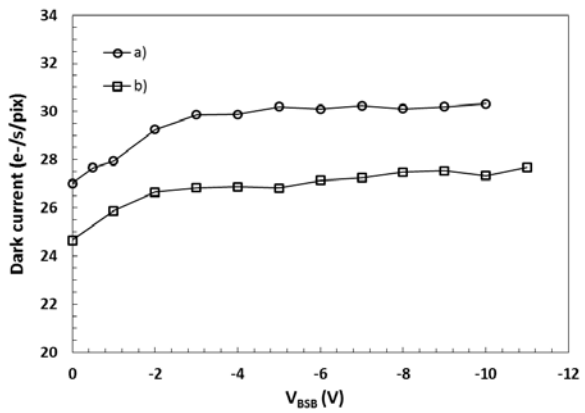

Fig. 6. Dark current at 23±1 °C as a function of the reverse bias for medium DDE (a) and deep DDE (b) 10 µm pixel arrays.

the onset of full depletion due to the nearly full suppression of surface dark current in PPD devices. As the depletion increases in depth it reaches the backside interface with the p^{++} substrate and cannot increase anymore; at this point the bulk dark current is expected to level off.

Fig. 6 shows the measured dark current in two pixel array variants as a function of the backside bias. The data is consistent with the expectation of full depletion, and the observed dark current is typical for the technology.

Presently the devices are being processed for BSI at e2v Technologies and the results from their characterization will be presented in due course.

IV. Conclusion

In this letter we present the first experimental results from a new PPD pixel design using an additional deep implant to create a potential barrier under the in-pixel p-wells, which effectively prevents parasitic substrate current flow when reverse bias is applied. The first device prototypes demonstrate that this principle, termed “deep depletion extension”, works as predicted by previous simulations and eliminates the leakage current. The device is able to reach reverse bias levels above what is required to achieve full depletion, and maintains its reverse current performance under illumination. The proposed pixel architecture promises to realize fully depleted devices with much improved QE in the near-infrared and soft X-ray bands, when thick high resistivity substrates are used.

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