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Optimal digital correlated double sampling for CCD signals

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The noise performance of digital correlated double sampling (DCDS) for readout of charge coupled devices (CCD) with dominant white noise is presented. The trade-offs between analogue and digital signal filtering and the impact on the sampling rate are investigated and numerically simulated for realistic systems. The results can be used to select the signal bandwidth, the settling accuracy and the ADC sampling rate for optimal DCDS noise performance.

**Introduction:** Digital correlated double sampling (Digital CDS, DCDS) is finding increasing use in high performance CCD camera systems, displacing traditional analogue techniques such as dual slope integration and clamp-and-sample. The main advantage of a DCDS system is the flexible configuration for different readout rates without component changes while maintaining sensor-limited noise performance. Its ability to suppress burst noise and electromagnetic interference by “blanking” of selected signal portions can also be valuable. In addition, sophisticated signal processing techniques for suppression of 1/f noise become possible.

The DCDS technique oversamples the CCD output signal in order to obtain and subtract the optical signal level from the reset level. This is essential for eliminating the reset noise, and allows further noise reduction by digital signal processing. It has been shown [1-2], that for white noise dominated systems the differential averaging, also known as the ideal dual slope integrator, is the optimal noise reduction method because it is a “matched filter” for CCD signals and results in the highest signal-to-noise ratio. In the digital domain the CDS is implemented by averaging sufficient number of samples of the signal and the reset levels, followed by their subtraction [3].

**Noise analysis:** The assumption of predominantly white noise is valid for the majority of CCD systems today. Modern CCDS, employing buried channel source follower output, show dominant white noise at reasonably fast readout rates; 1/f noise starts to become significant and the system power transfer function becomes

\[
|H_{DA}(f)|^2 = \frac{4\sin^2(\pi f t_{set})\sin^2[(N + M)\pi f t_{set}]}{N^2}\sin^2(\pi f t_{set})[1 + (2\pi f t_{set})^2]
\]

When \( t_{set} \to 0 \), corresponding to infinite bandwidth, the settling time \( t_{set} \) and the number of samples \( M \) approach zero. If we let \( N \to \infty \) then (4) becomes the power transfer function of the ideal dual slope integrator [2,4]:

\[
|H_{DL}(f)|^2 = \frac{4\sin^4(\pi f t_{set})}{(\pi f t_{set})^2}
\]

The integration time \( t_{int} \) is the maximum available time, given by:

\[
t_{int} = N t_s = T/2
\]

The output RMS noise of the ideal dual slope integrator \( V_{DS} \) can be found by integrating (5) for constant CCD white noise density \( e_{CCW} \)

\[
V_{DS} = \left( \int_0^{T} e_{CCW}^2 |H_{DA}(f)|^2 df \right)^{1/2} = e_{CCW}\sqrt{2/\pi}
\]

The expression (7) gives the lowest possible noise from a CDS processor. Other sources of noise, such as amplifier and ADC quantisation noise are assumed to be negligible, as should be the case in a well-designed system.

A real-world DA is characterised by \( t_{set} > 0 \) and finite number of samples \( N \). Higher \( t_{set} \) increases the amount of analogue filtering at the expense of less digital filtering, as the number of samples \( N \) decreases due to the longer settling time. Similarly to (7), the output RMS noise of the differential averager can be calculated by integrating (4) numerically with the number of samples \( M \) and \( N \) determined from the following relationships:

\[
M = t_{int}/t_s
\]

\[
T = 2(N + M)t_s
\]

For a single pole low pass response \( t_{set} \) can be determined from the dominant time constant and the settling error \( \epsilon \):

\[
t_{set} = t_p \cdot \ln(1/\epsilon)
\]

Using (4), (8) and (9) we can calculate the output RMS noise \( V_{DA}(f) \) of the DA as a function of only 4 parameters: the signal bandwidth \( BW \), the settling error \( \epsilon \), the CCD clock frequency \( F_c \) and the ADC sampling frequency \( F_s \). It is important to note that the noise performance of the differential averager can only approach the ideal dual slope integrator, therefore calculating the noise ratio \( NR = V_{DA}/V_{DS} \) provides a convenient figure of merit.

**Results:** Fig. 2 shows the calculated \( NR \) for different settling errors as a function of the analogue bandwidth \( BW \) for a system with single pole low pass response, ideal AA filter and \( F_c=100 \text{MHz} \). The CCD clock frequency \( F_c \) is 1 MHz, which is a typical value for a wide range of applications. It can be seen that \( NR \) falls to within 5% of the ideal at \( BW=20\text{MHz} \) and \( \epsilon=0.1\% \), corresponding to \( N=45 \) samples. Increasing the system bandwidth further brings only a small improvement, and at \( BW=50\text{MHz} \) the noise is 1.8% above the theoretical minimum.

The calculation of \( NR \) can be used to select the optimal parameters for a DCDS system, given certain CCD clock frequency and settling error,
and can be an important design tool. In particular, the ADC sampling rate and the system bandwidth can have implications on the power consumption, the complexity and the cost of the system. In Fig. 3 the noise ratio is calculated for $F_s=40$ MHz. It can be seen that $NR$ is 5% from the optimum for $\epsilon=0.1\%$ at $BW=16$ MHz and $N=18$ samples. In this case an identical noise performance is achieved at 2.5 times lower ADC sampling frequency and slightly lower analogue bandwidth, which could be beneficial for the system design. If the requirements on the settling accuracy are relaxed (leading to sizable, but correctable gain error), good noise performance can be achieved at even lower BW and $F_s$. As a rule of thumb, $F_s$ has to be about 20 times larger than $F_c$ for $\epsilon=0.1\%$ and 10 times larger for $\epsilon=1\%$, if the noise performance is to be within 10% of the theoretical minimum.

As expected, the insufficient stop-band attenuation of the single pole response causes additional noise due to aliasing. The lowest noise is achieved at the optimal system bandwidth of 9 MHz, however the noise is still 18% above ideal.

For the two pole system without an additional AA filter the lowest noise is achieved in the bandwidth range between 7 MHz and 13 MHz. The noise is about 10% higher than ideal, and above 13 MHz begins to rise due to aliasing. This could be adequate for most applications and offers a good balance between noise performance and system complexity.

Fig. 2 Noise ratio DALP1/DS as a function of the settling error. The ADC sampling frequency is 100 MHz and an ideal AA filter is used. The right hand side axis shows the number of samples $N$.

Fig. 3 Noise ratio DALP1/DS for 40 MHz; ADC sampling frequency.

Given that the system is oversampled, it is worth investigating whether the overall system frequency response could be used as a substitute to the additional high performance AA filter. Depending on the cut-off frequency, the single or two pole low pass responses have to be applied with care due to possible aliasing and additional in-band noise due to insufficient stop-band attenuation.

Fig. 4 shows the noise ratio for systems with single and two pole low pass response (with equal poles) without an additional AA filter for $\epsilon=0.1\%$. The result is compared to identical systems using ideal AA filters. In the case of two pole low pass response the bandwidth is:

$$BW_{2-3dB} = \frac{1}{2\pi\tau_D} \sqrt{2^2 - 1},$$

and the settling time to 0.1% is $9.2\tau_D$. From (4), the power transfer function becomes:

$$|H_{DALP2}(f)|^2 = \frac{1}{N^2} \frac{4\sin^2(N\pi f_D)\sin^2((N + M)\pi f_D)}{\sin^2(\pi f_D)[1 + (2\pi f_D\tau_D)^2]^2},$$

(10)

(11)