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Mitigating charge spill-back induced image lag with a multi-level transfer gate pulse in PPD image sensors

J. Ivory^a, K.D. Stefanov^{*a}, A.D. Holland^a

^a Centre for Electronic Imaging, The Open University, Walton Hall, Milton Keynes, MK7 6AA, UK

ABSTRACT

A new method for minimizing image lag due to charge spill-back has been developed for pinned photodiode CMOS image sensors. The proposed method involves the use of multi-level transfer gate voltage during a single charge transfer period. Measurement results show that the new transfer process maintains the lower values for image lag at low signal levels that a high transfer gate voltage grants, whilst simultaneously preserving the later onset of spill-back dominated lag that a lower transfer gate voltage allows.

Keywords: CMOS, transfer gate voltage, charge spillback, image lag

1. INTRODUCTION

Pinned Photodiode (PPD) CMOS image sensors (CIS) are now the most widely used electronic imaging devices worldwide, with applications ranging from smartphone cameras to machine vision. The technological advancements made over the last two decades have brought them to the same or better performance level as their predecessor, the CCD. With inherent advantages over the CCD, such as higher frame rate, better radiation hardness and lower energy consumption, they are beginning to be used in scientific imaging such as ground- and space-based astronomy. They do however fall behind the CCD in some metrics, one of these being charge transfer inefficiency – known as image lag in CMOS sensors. Image lag occurs when a fraction of the photogenerated charge remains in the PPD after charge transfer has occurred, causing undesired persistence, which is particularly noticeable when a dark scene is imaged after a bright one.

1.1 Image Lag

In a PPD CIS, lag is generally considered as the incomplete transfer of electrons from the PPD to the Floating Diffusion (FD), via the Transfer Gate (TG) during readout. The TG forms a potential barrier to the photogenerated electrons in the photodiode during integration. This barrier is then lowered during readout to allow the electrons to be transferred to the FD. The FD acts as a capacitor, converting the charge packet to a voltage to be read out.

There are several factors which can influence lag, such as the pixel size and shape¹, transfer gate voltage², FD reset voltage³ and signal level⁴. Many novel designs in pixel architecture have sought to reduce the effects of lag⁵⁻⁷, with varying degrees of success. Image lag is more prominent in large pixels with high full well capacity, which tend to dominate high-performance scientific applications. Typical image lag in PPD CMOS sensors can be around or below 1% and can be particularly detrimental in demanding applications, where CCDs with charge transfer inefficiency of 10^{-5} per pixel are commonplace.

At low signal levels image lag is dominated by incomplete transfer of electrons, due to potential barriers or “pockets” in the transfer path⁸. At higher levels of illumination, the main source of lag is charge spill-back⁹, which also has an adverse effect on linearity¹⁰. Spill-back occurs when the number of electrons transferred to the FD is sufficiently large, such that the FD potential becomes comparable to that of the area under the TG. This causes any further electrons transferred to have no preference to being in either the FD or under TG. When TG is turned off after the charge transfer period, and its potential returns to the off state, any electrons present underneath it will spill into either the FD and be read as signal, or back into the PPD where they will be read as lag in the next image.

This is shown in Figure 1, where the solid black line is the potential when the transfer gate is held high for signal transfer. The dashed line represents the moment the gate potential is reduced to V_{TGL} at the end of the charge transfer, allowing electrons present under the TG to spill in either direction. Here V_P is the pinning voltage of the photodiode, V_{TGH} is the gate voltage applied during transfer and V_{FD} is the reset voltage at the floating diffusion.

From Figure 1 it can be seen that increasing V_{TGH} will reduce the number of charges needed to bring the potential on the floating diffusion to the same level as under the transfer gate, lowering the signal level at which spill-back occurs. Lowering V_{TGH} will increase the signal level at which spill-back occurs, at the cost of a lower potential gradient with which to draw electrons across the TG at lower signals, increasing the image lag before it becomes spill-back dominated. A larger V_{FD} will also increase the signal at which spill-back occurs¹¹, but very often it is not possible to raise V_{FD} sufficiently due to supply voltage limitations and the threshold voltage of the reset transistor.

Figure 1. Potential diagram within a PPD pixel showing charge transfer when the transfer gate is high and spill-back when the gate returns to the low state.

1.2 Reducing charge spill-back

One method for reducing charge spill-back is introducing a doping gradient under TG in order to avoid the potential step between the PPD and the FD^{12, 13}. When the TG is on, this creates a potential gradient, causing the right hand side of the TG (Figure 1) to be more attractive to the transferring electrons than the left hand side.

The method proposed in this paper is to use more than one V_{TGH} level in a single transfer period. At the beginning of the transfer period V_{TG} is at its maximum, V_{TGH} , allowing for quick transfer of the photogenerated electrons. After this, the transfer gate is supplied a lower voltage for the rest of the transfer period, V_{TGM} . The lower voltage allows more electrons to transfer to the FD due to the increased potential difference between the TG and FD, reducing the number of electrons that may spill back into the PPD. The advantage to this over new pixel designs is that it can be readily implemented on virtually any CMOS sensor with just a minor software or hardware change.

2. DEVICE SIMULATION

Simulations of the device were done in Silvaco Atlas TCAD software¹⁴ to probe the movement of electrons during the charge transfer process. Multiple transfer gate voltages were investigated, including single level and two-level.

Figure 2 shows the density of electrons at the end of the transfer process in simulations for two V_{TGH} levels. The figure shows the density of electrons at the end of the transfer process, while the transfer gate is still high. In Figure 2(a) $V_{TGH} = 3.6$ V and the electrons have spread into the area of higher potential under the transfer gate itself, through to the side closest to the photodiode. Once the transfer gate is turned off and the potential returns to zero, the electrons on the photodiode side of the transfer gate are likely to spill back into the photodiode, resulting in image lag.

At $V_{TGH} = 2.7$ V (Figure 2 (b)) there are almost no electrons under the TG. When the transfer gate is turned off, the signal electrons will remain in the floating diffusion.

Figure 2. Simulated electron distribution under the TG at the end of the transfer period: (a) at $V_{TGH} = 3.6$ V, (b) at $V_{TGH} = 2.7$ V. Charge can be seen spreading out from the floating diffusion and under the transfer gate at the higher voltage. The legend shows the logarithm of the electron concentration in cm^{-3} .

Further simulations showed that lowering the reset voltage applied to the floating diffusion before charge transfer gives similar results to having a high V_{TGH} – a higher concentration of electrons on the photodiode side of the transfer gate at large signals. This further supports the theory that the cause of the spread of electrons is due to a decrease of electrical potential in the floating diffusion due to increased charge transferred to it.

3. EXPERIMENTAL RESULTS

3.1 Test setup

The sensor used in these tests is a PPD CMOS sensor designed at the Open University¹⁵. The chip contains 4 sections of 16×32 , 4T, $10 \mu\text{m}$ square pixels, with all tests run on one section only. The pixel architecture is standard in terms of PPD and TG shape, with a rectangular PPD $8.9 \mu\text{m}$ wide and $7.89 \mu\text{m}$ long and rectangular TG measuring $1.245 \mu\text{m}$ wide and $3.595 \mu\text{m}$ long. Illumination is provided by a LED with peak wavelength of 624 nm , and with a pulse width controlled via software. The modifications made to the external circuitry to allow for multiple transfer voltages in a single transfer pulse are shown in Figure 3.

Figure 3. Circuit diagram of modifications made to the camera board to achieve both the two-level and decaying V_{TG} . Switch 1 allows the transition between the two V_{TG} levels. Diodes 1 and 2 combined with the $11 \text{ k}\Omega$ variable resistor facilitate the voltage decay method. Switch 2 allows for the voltage decay circuitry to be bypassed. Switches 1 and 3 are both controlled electronically via software.

The switching performed by the ADG419 analogue switch allows for a very fast transition between the two supply voltages to the transfer gate. Using this switch whilst SW2 is closed results in a two-level transfer gate pulse, shown in Figure 4 as a solid black line.

With SW2 kept open the RC circuit serves to slow the transition between V_{TGH} and V_{TGM} . This creates an exponentially decaying waveform, showing in Figure 4 as a dashed red line.

Figure 4. Example waveforms applied to the transfer gate in this paper. T1 is the same for all regimes, whilst in T2 the dashed line represents a normal single level readout, the solid line a two-level readout and the red dashed line a decaying voltage.

For lag measurements, the sensor is illuminated with the LED at a constant brightness with variable on-time, while the sensor integration time remains constant. After signal integration, two frames are read out with no illumination between them – the first being the image and the second containing the lag signal. This is performed 100 times for each LED illumination time, and the mean of these 100 frames taken as the raw data. A mean dark frame of the same integration time is then subtracted from the lag data to remove any offsets. All tests are done at room temperature, and at a readout rate of 10 frames per second.

3.2 Standard readout results

To test the effect of V_{TGH} and V_{FD} experimentally, measurements were carried out whilst changing the two voltages separately. Figure 5 shows the results of varying V_{TGH} .

We observe that as V_{TGH} is decreased, the FD can collect more electrons before the potential reaches that of the TG, thus increasing the signal at which spill-back begins to dominate. At $V_{TGH} < 2.7$ V, the potential under TG is not high enough and so the lag is much higher than at the higher V_{TGH} voltages shown here. At smaller lag levels it becomes apparent that although the lower V_{TGH} results in a later onset of spill-back dominated lag, the lag values at lower signal levels - where lag is charge diffusion dominated - are greater than those at a higher V_{TGH} .

Figure 5. Measured image lag at a range of V_{TGH} using a normal single-level TG clock pulse.

Figure 6 demonstrates how varying the reset level on FD affects the signal at which spill-back occurs. As the V_{FD} is lowered, the spill-back occurs at lower signal values due to the decreased voltage difference between V_{TGH} and V_{FD} . With a lower voltage difference, fewer electrons are required to make the voltages equal, thus causing spill-back at lower signal levels.

Figure 6. Measured image lag at a range of V_{FD} with $V_{TGH} = 3.3$ V.

3.3 Multi-level readout results

Results in Figure 7 show that the multi-level TG voltage has the benefits of low image lag equal to that of $V_{TGH} = 3.3$ V until the knee-point, after which it closely follows the lowest lag achieved at $V_{TGH} = 2.7$ V. It was found that a short T1 at a high voltage followed by a long T2 at a lower voltage gave the best results. The high V_{TGH} allows fast movement of charge at the beginning of the transfer period, whilst a low V_{TGM} increases the potential difference between the floating diffusion and transfer gate. The lower TG voltage at the end of the transfer period follows the decreasing FD potential and ensures that fewer electrons remain under the gate when the transfer is stopped.

Ideal operating parameters were found to be around $V_{TGH} = 3.3$ V and $V_{TGM} = 2.7$ V. Image lag for $V_{TGM} < 2.7$ V increased due to the voltage approaching the threshold voltage of the transfer gate, which is about 2.6 V.

Figure 7. Image lag measured using a two-level transfer regime. Single level transfers at $V_{TGH} = 3.3$ V and 2.7 V are shown for comparison.

In addition to the two-level voltage method, further measurements were taken where the transition between V_{TGH} and V_{TGM} was an exponential decay instead of an abrupt change as shown in Figure 4. The time constant was chosen to be sufficiently long so that the TG voltage at the end of T2 does not fall below the threshold for charge transfer.

Figure 8 shows the results for the decaying voltage measurements alongside those of the multi-level and standard single level methods. Like the multi-level method, the exponentially decaying voltage has the advantages found in both the high and low single level transfer voltages.

Figure 8. Comparison of image lag measured with the three transfer gate voltage regimes discussed in this paper.

4. CONCLUSIONS

Through measurements of the image lag as a function of both the V_{TGH} and the potential at the floating diffusion after reset, results obtained support the theory that charge spillback dominates image lag at higher signal levels. By showing that a high transfer gate voltage or a lower reset voltage decreases the lag full well, these parameters are important factors to consider when trying to reduce the image lag. Whilst a high voltage on the transfer gate may be beneficial at small signals in low light conditions, a lower voltage may be more pertinent in images captured with more light or longer integration times.

The two-level transfer gate technique has shown that the effects of charge spill-back can be reduced by altering the TG potential during transfer. The change allows electrons under the gate to more favourably spill into the floating diffusion and therefore decrease the risk of them returning to the photodiode once the gate is turned off. The results have shown that with two-level transfer gate voltage, the benefits of both are seen, namely lower lag at both small and large signals.

The results using decaying V_{TGH} showed a further small reduction in lag at higher signal levels when compared to the two-level V_{TG} . Ideally this method of controlling the transfer voltage would be used in every situation to minimise the image lag, although it is harder to implement than the two-level regime as it requires tuning of the RC circuit decay time.

An important advantage of the described method is that it can be applied to many PPD image sensors with a simple change to their external drive electronics. It may also be used alongside other lag reduction techniques, such as increasing V_{FD} . It can also be used in sensors with a high dynamic range, as both dark and bright pixels will have their image lag reduced.

REFERENCES

- [1] Shin, B., S. Park, and H. Shin, "The effect of photodiode shape on charge transfer in CMOS image sensors," *Solid State Electronics* 54(11), 1416-1420 (2010).
- [2] Lofthouse-Smith, D.-D., et al., "Image lag optimisation in a 4T CMOS image sensor for the JANUS camera on ESA's JUICE mission to Jupiter," *Proc. SPIE* 10709, 107091J (2018).
- [3] Han, L., Yao, S. and Theuwissen, A., "A charge transfer model for CMOS image sensors," *IEEE Transactions on Electron Devices* 63(1), 32-41 (2015).
- [4] Wang, F., Han L., and Theuwissen, A., "Development and Evaluation of a Highly Linear CMOS Image Sensor with a Digitally Assisted Linearity Calibration," *IEEE Journal of Solid-State Circuits*, 53(10), 2970-2981 (2018).
- [5] Liu, W., et al., "Design of Novel Pixel with Non-Uniform Doped Transistor Channel and Triangle-Tooth Shape Pinned Photodiode for High Speed CMOS Image Sensors," *International Journal of Electronics and Electrical Engineering*, 114-120 (2017).
- [6] Cao, Z., et al., "Process techniques of charge transfer time reduction for high speed CMOS image sensors," *Journal of Semiconductors* 35(11), 114010 (2014).
- [7] Xu, Y. and Theuwissen, A.J., "Image lag analysis and photodiode shape optimization of 4T CMOS pixels," *Proc. Int. Image Sensor Workshop* (2013).
- [8] Liu, J., et al., "Simulation and measurement of total ionizing dose radiation induced image lag increase in pinned photodiode CMOS image sensors," *Nuclear Instruments and Methods in Physics Research A* 856, 32-35 (2017).
- [9] Michelot, J., et al., "Effects of Transfer Gate Spill Back in Low Light High Performances CMOS Image Sensors," *Photon Counting, Low Flux and High Dynamic Range Optoelectronic Detectors Workshop* (2016).
- [10] Bonjour, L.-E., Blanc, N., and Kayal, M., "Experimental Analysis of Lag Sources in Pinned Photodiodes," *IEEE Electron Device Letters* 33(12), 1735-1737 (2012).
- [11] S Xu, J., Wang, R., Han, L. and Gao, Z., "Analysis and Modeling of Spill Back Effect in High Illumination CMOS Image Sensors," *IEEE Sensors Journal* 20(6), 3024-3031 (2020).
- [12] Rizzolo, S., et al., "Influence of Pixel Design on Charge Transfer Performances in CMOS Image Sensors," *IEEE Transactions on Electron Devices* 65(3), 1048-1055 (2018).
- [13] Li, Y., et al., "Charge transfer efficiency improvement of a 4-T pixel by the optimization of electrical potential distribution under the transfer gate" *Journal of Semiconductors* 33(12), 124004 (2012).
- [14] Atlas TCAD simulation software, Silvaco Inc. (2016).
- [15] Stefanov, K.D., Clarke, A.S., Ivory, J. and Holland, A.D., "Design and Performance of a Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias," *Sensors* 18(118), (2018).