Open Research Online
The Open University’s repository of research publications
and other research outputs

CMOS image sensor

Patent
How to cite:

For guidance on citations see FAQs

© 2015 Konstantin Stefanov
Version: Version of Record
Link(s) to article on publisher’s website:

Copyright and Moral Rights for the articles on this site are retained by the individual authors and/or other copyright owners. For more information on Open Research Online’s data policy on reuse of materials please consult the policies page.

oro.open.ac.uk
A CMOS image sensor 101 comprises an active layer 11 of a first conductivity type arranged to be reverse biased and a pixel 20 comprising a photosensitive element comprising a well 22 of a second conductivity type and a well 21 of the first conductivity type containing active CMOS elements for reading and resetting the photosensitive element. The CMOS image sensor further comprises a doped buried layer 111 of the second conductivity type in the active layer beneath the well of the first conductivity type. The buried layer is arranged to extend a depletion region below the well of the second conductivity type also below the well of the first conductivity type.
This invention relates to a CMOS image sensor and an apparatus comprising the CMOS image sensor.

BACKGROUND

Silicon CMOS image sensors for imaging from infrared to soft x-rays are known. Figures 1 to 3 show equivalent circuit diagrams of known silicon CMOS image sensors using a photodiode, a pinned photodiode and photogate respectively, in which, T1 is a reset transistor, T2 is a source follower, T3 is a row select transistor and T4 is a transfer gate. Figures 4 to 7 show corresponding cross-sections of known CMOS image sensors using a photodiode, a buried photodiode, a pinned photodiode and photogate respectively.

However, to form near-infrared images it is desirable to use a relatively thick silicon active layer, e.g. 100-200 \( \mu \text{m} \), to provide sufficient absorption depth for the infrared radiation. It is known to apply a reverse bias across an active layer of CMOS image sensors to reduce crosstalk and improve quantum efficiency. However, because of the low operating voltages of CMOS image sensors, achieving full depletion can be very difficult for thick active layers e.g. over 20 \( \mu \text{m} \) and requires additional reverse biasing of the substrate. The thickness of an active layer of a CMOS image sensor is determined by the available voltage and silicon resistivity. For the highest available resistivity in CMOS currently available of approximately 1,000 ohm.cm for epi and with a 3.3V supply, a "thick" active layer means an active layer with a thickness approx. 1,000 ohm.cm for epi and with a 3.3V supply, a "thick" active layer means an active layer with a thickness that cannot be depleted under normal operating voltages - this corresponds to a thickness >20 \( \mu \text{m} \) or thereabouts. That is, currently full depletion with a 3.3V diode bias can be obtained only up to a thickness of approximately 18 \( \mu \text{m} \) with epi. In the case of bulk silicon the highest available resistivity is 10,000 ohm.cm and this could deplete up to around 50 microns. In either case, for greater thicknesses, depletion regions may be formed only under the photodiodes which would decrease quantum efficiency and cause crosstalk due to charge diffusion and slow charge collection. The applied reverse bias voltage may then cause a parasitic current to flow through the active layer around the depletion regions.

As shown in Figures 10 and 11, the extent of the overlap of the depletion regions creating the pinch-off is dependent on relative doping levels and depths of the p-wells and n-wells. Referring to Figure 10, with identically doped p wells 211 and n wells 221 of equal depth, and with the width \( L_{\text{nw}} \) of the n well 221 greater than a width \( L_{\text{pw}} \) of the p well 211, the depletion regions 151 and 161 may overlap to form a pinch off 171. Referring to Figure 11, with identically doped p wells 212 and n wells 222 but with the n wells 222 deeper and wider than the p wells 212, a greater overlap may occur between the n wells 222 and the p wells 212, allowing a parasitic current to flow.

Thus, a pinch-off 17 cannot be achieved under all operating conditions and may not be possible if the wells are deep or more highly doped than the photosensitive elements.

Although these effects have been described in a CMOS image sensor with a p-type substrate, it will be understood that the same effects occur in a CMOS image sensor with opposite conductivity type layers and wells.

The photodiode region and a transistor region. An n-type buried layer, which may be horizontal or U-shaped, is formed in the p-type substrate below the transistor region to prevent the bias voltage affecting the transistor region.

US 2008/0217723 discloses a back-illuminated CMOS sensor in which a back bias voltage is varied to vary a width of a depletion area in the photodiode to adjust the sensitivity of the sensor to red, green and blue light without using a colour filter. The CMOS sensor has a photodiode region and a transistor region. An n-type buried layer, which may be horizontal or U-shaped, is formed in the p-type substrate below the transistor region to prevent the bias voltage affecting the transistor region.
In accordance with the present invention there is provided a CMOS image sensor comprising: an active layer of a first conductivity type arranged to be reversed biased and a pixel comprising: a photosensitive element comprising a well of a second conductivity type; and a well of the first conductivity type containing active CMOS elements for reading and resetting the photosensitive element; and a doped buried layer of the second conductivity type arranged to extend a depletion region below the well of the first conductivity type also below the well of the second conductivity type. Advantageously, the doped buried layer is doped at substantially $10^{13}$ cm$^{-3}$ and the active layer has a doping level of $10^{13}$ cm$^{-3}$.

Conveniently, the doped buried layer is electrically floating.

Conveniently, a width of the doped buried layer of the second conductivity type is substantially equal to a width of the well of the first conductivity type.

Advantageously the CMOS image sensor comprises a plurality of pixels as described above and a guard ring comprising a well of the second conductivity type at least substantially encircling the plurality of pixels.

Conveniently, the pixel is on a front face of the substrate and the CMOS image sensor is arranged for illumination on the back face thereof, opposed to the front face.

Conveniently, the CMOS image sensor further comprises a contact on the back face arranged for applying the reverse bias to the CMOS image sensor.

Alternatively, the CMOS image sensor further comprises a contact on the front face arranged for applying the reverse bias to the CMOS image sensor.

According to a further aspect of the invention, there is provided an apparatus comprising a CMOS image sensor as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are further described hereinafter with reference to the accompanying drawings, in which:

Figure 1 is an equivalent circuit diagram of a known CMOS image sensor using a photodiode or buried photodiode;

Figure 2 is an equivalent circuit diagram of a known CMOS image sensor using a pinned photodiode;

Figure 3 is an equivalent circuit diagram of a known CMOS image sensor using a photogate;

Figure 4 is a cross-section diagram of the known CMOS image sensor of Figure 1 using a photodiode;

Figure 5 is a cross-section diagram of the known CMOS image sensor of Figure 1 using a buried photodiode;

Figure 6 is a cross-section diagram of the known CMOS image sensor of Figure 2 using a pinned photodiode;

Figure 7 is a cross-section diagram of the known CMOS image sensor of Figure 3 using a photogate;

Figure 8 is a cross-section diagram of a known CMOS image sensor with equal depth p wells and n wells;

Figure 9 is a cross-section of the known CMOS image sensor of Figure 8 showing variations in the extent of a depletion zone;

Figure 10 is a cross-section of a known CMOS image sensor with identically doped but unequal depth p wells and n wells;

Figure 11 is a cross-section of a known CMOS image sensor with identically doped equal depth p wells and n wells;

Figure 12 is a cross-section diagram of a CMOS image sensor according to the invention with buried layers substantially the same width as the p-wells;

Figure 13 is a cross-section diagram of a CMOS image sensor according to the invention with buried layers wider than the p-wells;

Figure 14 shows potential contours within an active layer of a CMOS image sensor with a single buried layer;

Figure 15 shows current density contours within the active layer of the CMOS image sensor of Figure 14;

Figure 16 is a graph of potential versus distance along the cutline 1 of the CMOS image sensor of Figure 14;

Figure 17 is a graph of potential versus distance along the cutline 2 of the CMOS image sensor of Figure 14;

Figure 18 is a cross-section diagram of a CMOS image sensor according to the invention comprising a photodiode;

Figure 19 is a cross-section diagram of a CMOS im-
age sensor according to the invention comprising a buried photodiode;
Figure 20 is a cross-section diagram of a CMOS image sensor according to the invention comprising a pinned photodiode;
Figure 21 is a cross-section diagram of a CMOS image sensor according to the invention comprising a photogate;
Figure 22 is a schematic diagram of an apparatus comprising an image sensor according to the invention; and
Figure 23 is a schematic diagram of a night vision apparatus comprising an image sensor according to the invention.

DETAILED DESCRIPTION

[0024] Referring to Figure 12, a pinned photodiode CMOS back-illuminated image sensor 101, according to the invention, comprises a p+ substrate or backside contact 12 on which is a p- epitaxial or bulk active layer 11. Pixels 20 each comprising a photodiode located in an n+ well 22 and active devices for reading charge from the photodiode and resetting the photodiode in a p-well 21 on a front face of the epitaxial or bulk layer 11. A guard ring in the form of an n+ well 23 surrounds the plurality of pixels 20. A substrate bias contact is supplied by a p+ well 24 on the front face of the epitaxial or bulk layer 11 at a distance from the guard ring of at least the thickness of the active layer (Figure 12 is not drawn to scale). Floating buried lightly doped n-layers 111, doped at, for example, 10^15 cm^-3 compared with typical doping levels of 10^13 cm^-3 for the active layer, are located beneath the p-wells containing the active devices. The depth of the buried n- implant is typically 2 to 3 µm, sufficient for the buried layer to be deeper than a depth of the p-well which is 0.5 to 1.5 µm deep, the same as the photodiode. Peak p-well concentration is 10^16, 10^17 cm^-3. The buried n- implant is shown approximately a same size as the p-well, but could be wider than the p-well. It is envisaged that the buried n- implant could be extended to be in weak contact with the photodiodes and not electrically floating.

[0025] A peak diode potential of a pinned photodiode is determined by doping levels of the diode and the pinning implant and is in the range of 1V to 2V for a 3.3V supply. The potential must not be so low as to limit full well capacity or so high as to make charge transfer slow and cause image lag. With a large capacitance diode the potential change at full well is of the order of 0.5V.

[0026] In a pinned photodiode structure with a floating diffusion layer between a transfer gate and a reset gate, the floating diffusion depleton should be fully contained within the p well otherwise the floating diffusion layer will compete for charge with the diode. This determines the doping and depth of the p well for a fixed floating diffusion voltage. The p well should be deeper than the shallow trench insulation, which typically has a depth of 0.31 µm. The p well is preferably deeper than the diode implant which increases the problem of reducing the substrate current. From studies with identical diode and p well doping, the p well width should be less than 2 µm.

[0027] It will be understood that the buried n- layer may be implanted using an ion beam of sufficiently high energy. If a typical manufacturing process for CMOS image sensors is assumed, the new implant requires only one additional step. In one implementation the buried n-layer is implanted before or after the p-well, using a same mask for alignment with the p-well. In another implementation the buried n-layer is implanted before or after the p-well using a different mask. In this case the new n- implant can have a different size from the p-well. Implantation before the p-well is preferred to avoid affecting parameters of transistors in the p-well.

[0028] Figure 13 shows a pinned photodiode CMOS back-illuminated image sensor 101', according to the invention, similar to the image sensor 101 of Figure 12, but in which the buried n-layer 111' is wider than the p-well 21.

[0029] Figure 14 shows a simulation of potential contours of the CMOS image sensor of Figure 12, in which the contour lines are at 1 V intervals. The potentials on the diodes D1 and D2 are set to 1.5V to match actual potentials in a four-transistor pinned photodiode. In this simulation, the p-type epitaxial or bulk layer doping is 10^13 cm^-3, providing a resistivity of approximately 1 KOhm.cm. The doping of the n- implant is approximately 10^15 cm^-3. If it is lower (10^14 cm^-3) it is ineffective because pinch-off does not occur, and if higher (10^16 cm^-3) a potential pocket is formed at the implant location. The doping of the photodiode is approximately 10^16 cm^-3, and this sets the upper limit for the n- implant, above which a potential pocket is formed. The n- implant 111 has a depth of approximately 1 µm and is not in significant contact with the p-well, so that the p-well and the n- implant can be considered independent.

[0030] Figure 15 shows a hole current density with contours ranging on a logarithmic scale from 10^2 A/cm^2 to 10^5 A/cm^2, corresponding to the potential contours of Figure 14. A pinch-off is maintained where there is a lightly doped n-type floating buried layer 111 under the p-well 2 but the pinch-off is open, allowing a current to flow, under the p-well 3 with no corresponding buried n-layer. It may be that charge carriers are diverted to travel along the length of the buried layer 111. The effect of the lightly doped n layers allows substantially larger bias voltages of say -20V to be applied to thick substrates of, for example, 100 - 200 µm without causing parasitic currents between the p wells and the back side contact where present or the front side bias p+ well, as the case may be. Thus, pinch-off is maintained at much lower photodiode voltages which occur when large signals have been collected, than in the prior art, or when the p-wells are highly doped or deep. The parasitic substrate current is much reduced or eliminated in the CMOS image sensor of the invention.

[0031] Figure 16 shows the potential 131 along the line 130 of Figure 14 showing a potential barrier 132 prevent-
ing conduction to the p-well 2 with the buried layer 111. However, this barrier does not prevent charge from reaching the photodiodes 22 to the sides of p-well 2 with the buried layer 111.

[0032] Figure 17 shows the potential 141 along the line 140 of Figure 14 showing that there is no barrier between the photodiode D2 and the n- implant 111 and that charge will collect at the photodiodes 22. A potential pocket is not formed.

[0033] Although these effects have been described in a CMOS image sensor with a p-type substrate, it will be understood that similarly a CMOS image sensor with opposite conductivity type layers and wells may be provided. It will also be understood that the invention can be applied to both back and front illuminated image sensors of a first conductivity type in which the photosensitive element comprises a well of a second conductivity type, such as image sensors comprising a photodiode, a buried photodiode, a pinned photodiode or a photogate.

[0034] Thus Figure 18 shows a cross-section of an image sensor 801 comprising photodiodes 822 and buried n- layers 811 below p wells 821. Otherwise the image sensor is similar to the prior art sensor of Figure 4.

[0035] Figure 19 shows a cross-section of an image sensor 901 comprising buried photodiodes 922 and buried n- layers 911 below p wells 921. Otherwise the image sensor is similar to the prior art sensor of Figure 5.

[0036] Figure 20 shows a cross-section of an image sensor 1001 comprising pinned photodiodes 1022 and buried n- layers 1011 below p wells 1021. Otherwise the image sensor is similar to the prior art sensor of Figure 6.

[0037] Figure 21 shows a cross-section of an image sensor 1101 comprising photogates 1122 and buried n-layers 1111 below p wells 1121. Otherwise the image sensor is similar to the prior art sensor of Figure 7.

[0038] Figure 22 is a schematic figure of an apparatus 500 incorporating an image sensor 501 according to the invention.

[0039] Figure 23 is a schematic figure of a night vision apparatus 600 comprising an objective lens 601 or other image forming means, an image sensor 601 according to the invention, a processing module for processing signals from the image sensor 601 for presentation on a display means 604.

[0040] It will be understood that in the described CMOS image sensor the active devices in the p well are protected by the p well from charge carriers generated in the epitaxial or bulk layer by incident electromagnetic radiation.

[0041] The image sensor of the invention has the advantage of being compatible with a CMOS manufacturing process. The invention requires only on additional processing step available in most CMOS manufacturing plants to create the floating buried deep implants of a type. The structures of the prior art require more and more expensive manufacturing steps than the present invention.

[0042] The invention has the advantage of completely avoiding interaction with the delicate structure of a pinned photodiode.

[0043] The invention has particular applications in night vision applications using a red glow of the night sky and in infrared and x-ray astronomy.

[0044] Throughout the description and claims of this specification, the words "comprise" and "contain" and variations of them mean "including but not limited to", and they are not intended to (and do not) exclude other moieties, additives, components, integers or steps. Throughout the description and claims of this specification, the singular encompasses the plural unless the context otherwise requires. In particular, where the indefinite article is used, the specification is to be understood as contemplating plurality as well as singularity, unless the context requires otherwise.

[0045] Features, integers, characteristics, compounds, chemical moieties or groups described in conjunction with a particular aspect, embodiment or example of the invention are to be understood to be applicable to any other aspect, embodiment or example described herein unless incompatible therewith. All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive. The invention is not restricted to the details of any foregoing embodiments. The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A CMOS image sensor (101) comprising:

   - an active layer (11) of a first conductivity type arranged to be reversed biased and a pixel (20) comprising:
   - a photosensitive element (22) comprising a well of a second conductivity type; and
   - a well (21) of the first conductivity type containing active CMOS elements for reading and resetting the photosensitive element; and
   - characterised by:
   - a doped buried layer (111) of the second conductivity type in the active layer beneath the well of the first conductivity type arranged to extend a depletion region below the well of the second conductivity type also below the well of the first conductivity type to form an extend-
ed depletion region in the active layer; wherein the extended depletion area in the active layer is arranged to pinch off a parasitic current path between the well of the first conductivity type containing active CMOS elements and a substrate or backside contact (12).

2. A CMOS image sensor as claimed in claim 1 wherein the doped buried layer is doped at substantially $10^{15}$ cm$^{-3}$ and the active layer has a doping level of $10^{13}$ cm$^{-3}$.

3. A CMOS image sensor as claimed in claims 1 or 2, when the doped buried layer is electrically floating.

4. A CMOS image sensor as claimed in any of the preceding claims, wherein a width of the doped buried layer of the second conductivity type is substantially equal to a width of the well of the first conductivity type.

5. A CMOS image sensor as claimed in any of the preceding claims, wherein a width of the doped buried layer of the second conductivity type is greater than a width of the well of the first conductivity type.

6. A CMOS image sensor as claimed in any of the preceding claims, further comprising a plurality of pixels as claimed in claim 1 and a guard ring comprising a well of the second conductivity type at least substantially encircling the plurality of pixels.

7. A CMOS image sensor as claimed in any of the preceding claims wherein the pixel is on a front face of the substrate and the CMOS image sensor is arranged for illumination on the back face thereof, opposed to the front face.

8. A CMOS image sensor as claimed in claim 7, further comprising a contact on the back face arranged for applying the reverse bias to the CMOS image sensor.

9. A CMOS image sensor as claimed in claim 7, further comprising a contact on the front face arranged for applying the reverse bias to the CMOS image sensor.

10. A CMOS image sensor as claimed in any of the preceding claims wherein the photosensitive element comprises one of a photodiode, a buried photodiode, a pinned photodiode or a photogate.

11. An apparatus (500) comprising a CMOS image sensor (501) as claimed in any of claims 1 to 10.

12. A night vision apparatus (600) comprising a CMOS
Fig. 4

Fig. 5
Fig. 8
(Prior Art)
Fig. 9
Prior Art
Fig. 10
Prior Art

Identically doped pwell and nwell

Fig. 11
Prior Art

Identically doped pwell and nwell (nwell is deeper)
Fig. 18

Fig. 19
<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document with indication, where appropriate, of relevant passages</th>
<th>Relevant to claim</th>
<th>CLASSIFICATION OF THE APPLICATION (IPC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>* paragraphs [0002], [0006], [0034] - [0039] * * figures 4, 5 * -----</td>
<td>6,12</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>US 2009/050998 A1 (MIURA TOSHIKI [JP]) 26 February 2009 (2009-02-26)</td>
<td>1,5,6,10</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>* paragraphs [0009], [0041] - [0047] * * figure 1 * -----</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>* paragraph [0006] * -----</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>EP 1 551 062 A2 (DONGBU ELECTRONICS CO LTD [KR]) 6 July 2005 (2005-07-06)</td>
<td>1,5,10, 11</td>
<td></td>
</tr>
<tr>
<td></td>
<td>* paragraphs [0050] - [0056] * * figure 4 * -----</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* column 7, lines 4-52 * * figure 2a * -----</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The present search report has been drawn up for all claims

Place of search: Munich
Date of completion of the search: 13 July 2015
Examiner: Markmann, Markus

**CATEGORY OF CITED DOCUMENTS**

- X: particularly relevant if taken alone
- Y: particularly relevant if combined with another document of the same category
- A: technological background
- O: non-written disclosure
- P: intermediate document
- T: theory or principle underlying the invention
- E: earlier patent document, but published on, or after the filing date
- D: document cited in the application
- L: document cited for other reasons
- &: member of the same patent family, corresponding document
This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td>US 2008217723 A1</td>
<td>11-09-2008</td>
<td>NONE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4979513 B2</td>
<td>18-07-2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2009049317 A</td>
<td>05-03-2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>KR 20090020476 A</td>
<td>26-02-2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TW 200924215 A</td>
<td>01-06-2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2009050998 A1</td>
<td>26-02-2009</td>
</tr>
<tr>
<td>US 2008142714 A1</td>
<td>19-06-2008</td>
<td>NONE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 1551062 A2</td>
<td>06-07-2005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4171723 B2</td>
<td>29-10-2008</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2005197646 A</td>
<td>21-07-2005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>KR 20050069083 A</td>
<td>05-07-2005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2005139752 A1</td>
<td>30-06-2005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP H11284168 A</td>
<td>15-10-1999</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 6211509 B1</td>
<td>03-04-2001</td>
</tr>
</tbody>
</table>

For more details about this annex: see Official Journal of the European Patent Office, No. 12/82
REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader’s convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

• US 20050139752 A [0009]