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A Global Shutter CMOS Image Sensor for Hyperspectral Imaging

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ABSTRACT

Hyperspectral imaging has been providing vital information on the Earth landscape in response to the changing environment, land use and natural phenomena. While conventional hyperspectral imaging instruments have typically used rows of linescan CCDs, CMOS image sensors (CIS) have been slowly penetrating space instrumentation for the past decade, and Earth observation (EO) is no exception. CIS provide distinct advantages over CCDs that are relevant to EO hyperspectral imaging. The lack of charge transfer through the array allows the reduction of cross talk usually present in CCDs due to imperfect charge transfer efficiency, and random pixel addressing makes variable integration time possible, and thus improves the camera sensitivity and dynamic range.

We have developed a 10T pixel design that integrates a pinned photodiode with global shutter and in-pixel correlated double sampling (CDS) to increase the signal to noise ratio in less intense spectral regimes, allowing for both high resolution and low noise hyperspectral imaging for EO. This paper details the characterization of a test device, providing baseline performance measurements of the array such as noise, responsivity, dark current and global shutter efficiency, and also discussing benchmark hyperspectral imaging requirements such as dynamic range, pixel crosstalk, and image lag.

Keywords: CMOS image sensor (CIS), hyperspectral imaging, correlated double sampling (CDS), global shutter, high speed imaging, low noise.

1. INTRODUCTION

Global shutter image sensors find numerous applications in areas where instantaneous whole image capture (snapshot) is essential to eliminate motion distortions, such as in high speed imaging and machine vision. Such sensors are suitable also for Earth observation from space, and are being considered for satellite hyperspectral cameras¹. Complementary Metal-Oxide Semiconductor (CMOS) global shutter imagers offer several advantages over conventional Charge Coupled Devices (CCD), such as improved radiation hardness, lower power requirements and high speed readout capabilities.

Most conventional 4T CMOS image sensors generally operate in a rolling shutter mode, and 5T designs add the ability to perform global reset and global snapshot². Practically all modern CIS designs are based on the pinned photodiode (PPD) structure³ due to its ability to perform efficient correlated double sampling (CDS) and eliminate the reset noise present in 3T designs. The dark current in PPD pixels is typically very low due to the suppression of interface dark current generation by surface pinning.

In rolling shutter mode the image frame is created from the sequential readout of each row from the sensor in turn, which can create significant motion artifacts. Global reset partially compensates for this by clearing the image signal at the same point of time for all pixels, but the finite sensor readout time adds increasing amount of integration time per row and therefore creates some motion blur.

Global shutter operation eliminates motion distortions by promptly and simultaneously capturing and storing the full image information from each pixel. 5T pixel designs can operate in global shutter mode by performing global reset, followed by an integration period and simultaneous transfer of all signal charges from the PPD to the sense node inside each pixel. This technique however, prevents the implementation of CDS because the reset noise remains, and the sensor exhibits higher readout noise. CDS in 5T pixel sensors can be implemented digitally by reading out the whole sensor once after reset and once more after the global shutter image capture, and subtracting the two values off-sensor. The drawback of this method is the overhead of two sensor readouts and the reduction of the frame rate, and also the less effective suppression of $1/f$ noise due to the large time difference between the samples.

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CDS is essential for low noise global shutter imaging, but its implementation increases pixel complexity and area because of the additional storage elements for the reset and the signal samples. Signal storage in the charge domain has been developed⁴ and has the important advantage of eliminating additional kTC noise from capacitor charging, at the expense of customized PPD design. Storage in the voltage domain across capacitors is somewhat easier to implement and many examples exist⁵⁻⁹, but storage capacitors may occupy a large part of the pixel and restrict the minimum pixel size and the fill factor.

Regardless of the storage mode, global shutter imagers implementing CDS need to address a number of design challenges, such as achieving high dynamic range and fill factor combined with low noise, high speed readout and good global shutter efficiency. Two-tier CIS with split detection and storage layers⁶ could be valuable in solving many of these challenges and offer improved performance in cases where the increased complexity can be justified.

This paper describes the design and the operation of a new 10T image sensor, the CIS109, featuring global reset, global shutter and per-pixel CDS. The CDS architecture⁵ is based on a circuit which eliminates some of the shortcomings of the 8T and 9T designs⁷⁻⁹ such as the capacitive division between the reset and signal samples. The main intended application is hyperspectral imaging for Earth observation, however the sensor is also applicable to other high speed imaging applications such as machine vision.

2. DEVICE DESIGN AND OPERATION

Pixel Design

The CIS109 device has two identical 188×50 pixel array blocks with pixel schematic shown in Figure 1. The pixel size is $14 \mu\text{m}$ square, of which the PPD occupies $7 \mu\text{m} \times 7 \mu\text{m}$, with the rest of the circuit filling the remainder of the pixel area. The chip was manufactured by TowerJazz Semiconductor using $0.18 \mu\text{m}$ image sensor CMOS process, featuring pinned photodiode (PPD) photosensitive elements, single poly and 4 metal layers. The device is front side illuminated.

The transistors M1-M5 together with the pinned photodiode form a traditional 5T pixel design. The gate RSTPD clears the charge stored in the PPD and can be used as a global reset when all rows are enabled. The gate TRA works as a charge transfer gate from the PPD to the floating diffusion (the sense node), where charge-to-voltage conversion occurs. The transistor M3 resets the floating diffusion to an external reference voltage. With the addition of M6-M10, the storage capacitors C1 and C2 and the reference voltage V_{REFRCDS} the pixel becomes capable of global shutter mode with per-pixel CDS. The transistor M7 is biased to maintain small standing current I_{PIX} for the first stage source follower M4. The source followers M4 and M9 are low noise transistors with reduced threshold voltage.

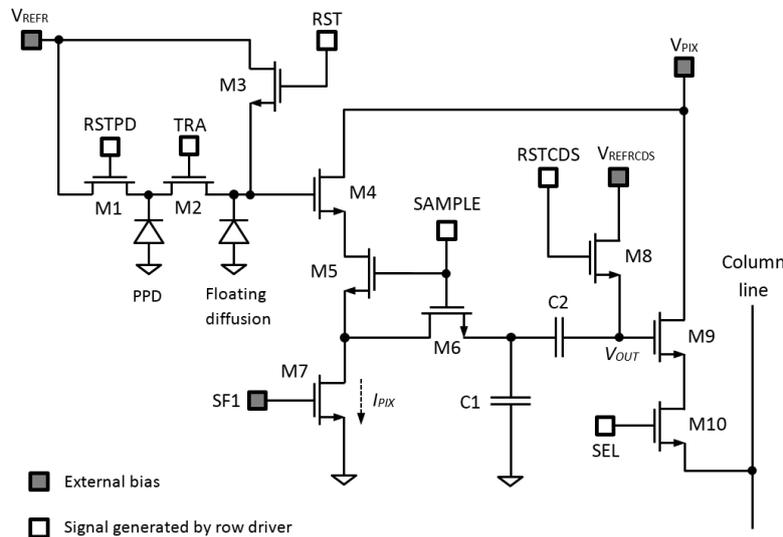


Figure 1. Simplified schematic of the CIS109 pixel.

Pixel Operation

Figure 2 shows the timing diagram of the pixel control signals during image integration and capture. Optical signal is integrated up to the moment of the charge transfer initiated by the TRA pulse. For global shutter operation all image rows should be selected, and the readout begins with the reset of the floating diffusion to the voltage V_{REFR} by M3. Both M3 and M8 are operated as linear switches by applying sufficiently high gate voltage to ensure hard reset of the nodes connected to their respective sources. After a floating diffusion reset, the transistors M5, M6 and M8 are switched on and the capacitor C1 is charged to

$$V_{C1} = V_{REFR} - V_T, \quad (1)$$

where V_T is the threshold voltage of M4. At the same time, the voltage across C2 becomes:

$$\Delta V_{C2} = V_{REFRCDS} - V_{C1} = V_{REFRCDS} - V_{REFR} + V_T. \quad (2)$$

After the end of the signal integration, the signal charge is transferred to the floating diffusion by driving the transfer gate TRA high. Next, the transistors M5 and M6 are switched on while M8 is kept off. The voltage on C1 becomes

$$V_{C1} = V_{REFR} - V_S - V_T, \quad (3)$$

where V_S is the voltage step at the floating diffusion generated by the signal charge. The voltage across C2 has not changed because M8 is not conducting, and the voltage at the gate of M9 V_{OUT} can be expressed as the sum of the voltages across C1 (3) and C2 (2), connected in series:

$$V_{OUT} = V_{REFR} - V_S - V_T + V_{REFRCDS} - V_{REFR} + V_T = V_{REFRCDS} - V_S. \quad (4)$$

The voltage V_{REFR} in (1), (2) and (3) contains the same sampled kTC noise component after floating diffusion reset, and CDS functionality is achieved due to the removal of V_{REFR} , and therefore of the reset noise as well, from the output signal V_{OUT} . When the row select transistor M10 turns on for pixel readout, the source follower M9 buffers V_{OUT} to the column output line. The image array restarts signal integration after the signal TRA is deactivated. If required, the whole sensor can be reset by clocking the RSTPD gate, as shown with a dashed line in Figure 2.

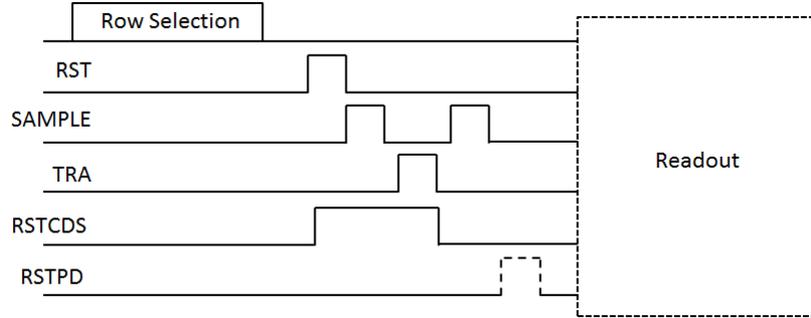


Figure 2. Timing diagram for signal integration and global shutter image capture.

Array Readout

The image array is read out in a column-parallel fashion with one serial output per block, as shown in the block diagram in Figure 3. The readout is simultaneous with the integration of the next image, as the signal from the image being read out is stored in the two pixel storage capacitors. The row shift register allows any number and combination of rows to be selected and enables the row control signals via the row buffer. The column shift register selects the signal from one column at a time to be connected to the output lines OUTS and OUTR.

The timing diagram of the pixel array readout is shown in Figure 4. After an image has been captured and the voltages V_{OUT} have been stored in every pixel simultaneously, the pixel array is addressed one row at a time via the row shift register, which generates the drive pulse SEL to the gates of M10. The stored V_{OUT} is sampled on the column signal

capacitors C_S by turning the switches SHS on while RSTCDS is low and the transistor M8 is off. The row is read out externally by multiplexing the signals on C_S to the output OUTS, controlled by the column shift register. The output voltage on OUTS is given by (4) with the addition of a fixed offset from the threshold voltage of M9 and the output buffer.

A second storage capacitor C_R is provided within the column circuitry for removal of V_{REFCDS} and the other fixed offsets in the readout chain. As shown in the timing diagram in Figure 4, it is possible to read out CIS109 in a mode where the CDS reference voltage is stored on C_R by turning M8 on simultaneously with the switch SHR. This resets the signal sample and therefore has to be done after the signal has been safely stored to C_S . The voltage stored across C_R is V_{REFCDS} and is subject to the same fixed offsets as the voltage on C_S with the exception of the offset of the output buffer. If the two output buffers have identical offsets, subtracting OUTS from OUTR gives a differential output signal which is simply V_s . The drawback of this readout mode is the increased noise from the column circuitry, but this is minor because the overall noise performance is dominated by the first stage source follower.

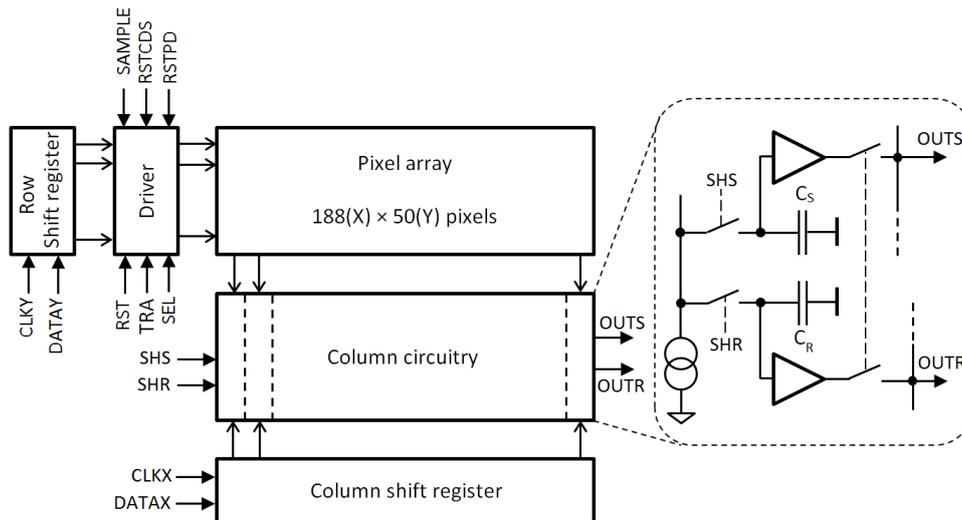


Figure 3. Block diagram of CIS109. The column readout circuitry is shown within dashed lines.

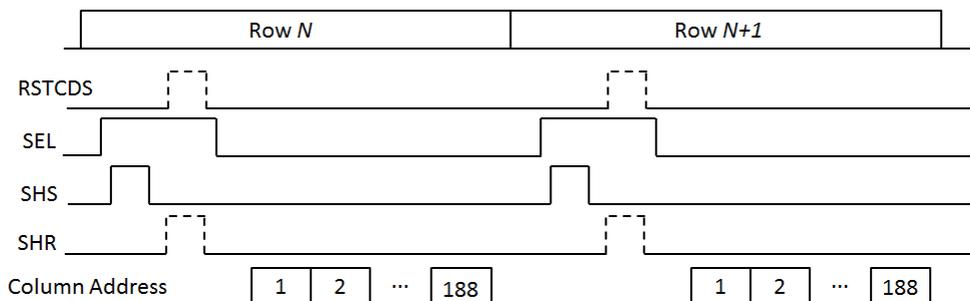


Figure 4. Timing diagram for array readout of CIS109.

3. EXPERIMENTAL RESULTS

A photograph of the CIS109 chip mounted in a PCB carrier is shown in Figure 5. The device was characterized in a laboratory setup allowing the generation of the necessary bias voltages, currents and clock signals according to the timing diagrams in Figure 2 and Figure 4. The light stimulus was provided by a red LED controlled by the readout sequence, and the output was digitized by a 16-bit differential ADC running at an effective sampling rate of 250 kpix/s. The device was operated in differential output mode as described in the previous section.



Figure 5. Photograph of CIS109 in a printed circuit board carrier.

Bias optimization

The operating biases and clock amplitudes of CIS109 were optimized in line with the transistor design parameters to achieve the maximum output signal and dynamic range. In particular, the storage capacitors C_1 , C_2 , C_S and C_R are realized as enhancement mode MOSFET gate capacitors and an appropriate bias to keep the channel in inversion at all times is required to prevent capacitance collapse. The required capacitor bias affects the rest of the pixel bias voltages.

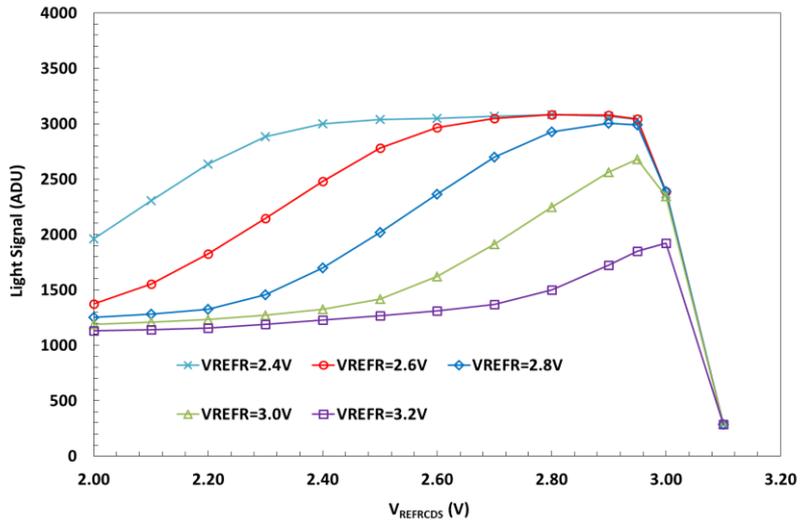


Figure 6. Light signal output as a function of the $V_{REFRCDS}$ for different V_{REFR} .

In order to maximize the dynamic range of the sensor, the reset voltage V_{REFR} and the CDS reference voltage $V_{REFRCDS}$ have to be as high as possible, while keeping the storage capacitors biased in inversion. The optimum values were found by scanning $V_{REFRCDS}$ and measuring the output sensor signal at fixed mid-range light stimulus and V_{REFR} . Figure 6 shows that the useful range of $V_{REFRCDS}$ is between 2.7 V to 2.9 V for V_{REFR} between 2.4 V and 2.6 V. Further device characterization was carried out using the bias and control signal values shown in Table 1, unless stated otherwise.

Table 1. Bias and control values for CIS109 characterization.

Bias or Amplitude	Value
V_{PIX}	3.2 V
V_{REFR}	2.6 V
$V_{REFRCDS}$	2.8 V
I_{PIX}	1 μ A
RST, RSTCDS	4.0 V
SAMPLE, SEL	3.3 V
TRA	2.6 V

Photoresponse and Linearity

Figure 7 shows the output signal of CIS109 as a function of the illumination time from a constant intensity LED. The maximum output voltage in saturation is 1.3 V. The linearity of the device was calculated by fitting a straight line to the photoresponse curve in Figure 7 up to 1.1 V output signal and subtracting the data from the fit to obtain the residuals. Fig. 8 shows the obtained linearity curve as a function of the output signal, normalized to the full scale range. The observed nonlinearity in CIS109 shows a characteristic “double hump”, which does not exist in a similar 4T PPD pixel using the same manufacturing technology¹⁰. This additional nonlinearity is attributed to the increased number of transistors in the pixel and the two storage capacitors.

The main device parameters were obtained using analysis of the Photon Transfer Curve (PTC)¹¹. The effectiveness of the global shutter and the parasitic light sensitivity of the device when an image has been stored in pixel was also studied, as this is an important parameter for high speed and hyperspectral imaging.

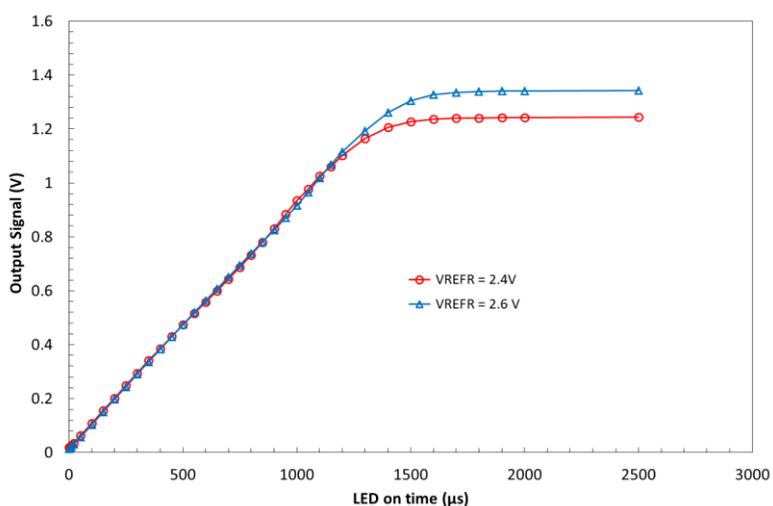


Figure 7. Output response of CIS109 with $V_{REFRCDS} = 2.8$ V.

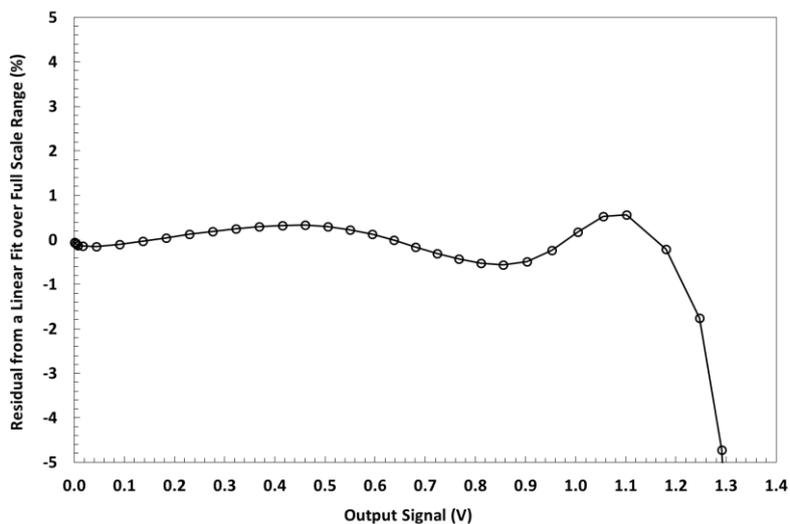


Figure 8. Linearity of the output response of CIS109.

Noise, Dark Current and Full Well Capacity

The system gain was obtained from the mean-variance plot¹¹ in Figure 9 by using the signal up to approximately 4500 Analog-to-Digital Units (ADU), which is the point where the signal variance begins to deviate from proportionality to the signal mean. The calculated system gain is $3.0 e^-/\text{ADU}$ and in our system $1 \text{ ADU} = 305 \mu\text{V}$.

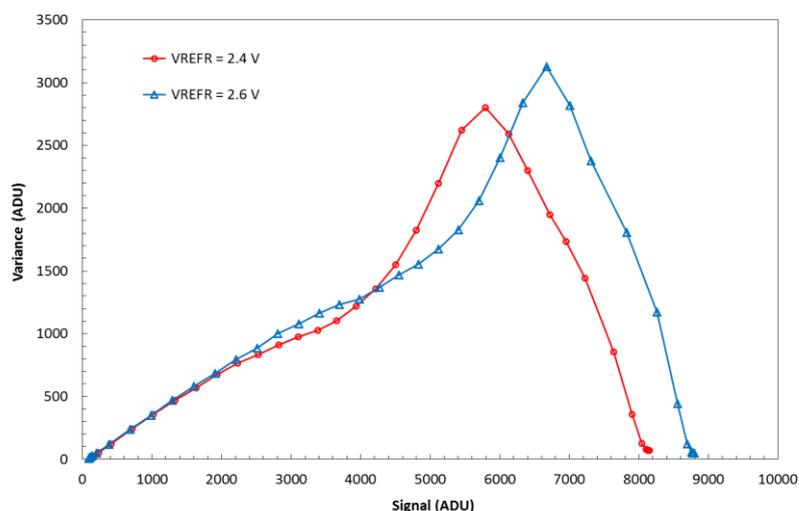


Figure 9. Mean-variance curve of CIS109 for two values of V_{REFR} and fixed $V_{\text{REFRCDS}} = 2.8 \text{ V}$. The higher signal capacity at higher V_{REFR} is clearly seen.

Based on the system gain and the off-sensor electronics gain of 2.0, the Charge-to-Voltage Factor (CVF) for CIS109 is $50.8 \mu\text{V}/e^-$ and the input-referred noise is $7.6 e^- \text{ RMS}$. Both values match well the simulated design parameters.

The measured dark current is $26.7 e^-/\text{pix.s}$ at $22 \pm 0.5 \text{ }^\circ\text{C}$, consistent with the typical values for this technology.

The Full Well Capacity (FWC), defined as the signal level where the sensor nonlinearity reaches 1% is $24.5 ke^-$. It is worth noting that the FWC determined from the onset of drop in signal variance (Figure 9), which is the most sensitive to any effects involving charge redistribution or signal limiting, is significantly lower, at $20 ke^-$. The saturation well capacity calculated from Figure 7 is $26 ke^-$. The FWC is entirely dominated by the readout circuitry and not the PPD, which has intrinsic carrier handling capacity above $50 ke^-$.

The dynamic range of the sensor, determined from the ratio of the saturation FWC and the readout noise is 3400:1, or 71 dB.

Image Lag

PPD image sensors suffer from image lag due to the weak electric field assisting charge transfer and the vulnerability to small potential barriers or pockets³. The image lag in CIS109 was measured by comparing the readout signal in a clock sequence with and without RSTPD reset after the global image capture (Figure 2). In the presence of image lag some charge remains in the PPD after the transfer to the sense node; it then adds to the photogenerated charge during the next exposure. However, a sufficiently long RSTPD pulse can clear the PPD and the next exposure will begin with zero stored signal. The effect is that the mean readout signal without RSTPD after the global capture is higher than in a sequence with the RSTPD pulse included.

Fig. 10 shows the image lag measured by this method as a function of the stored signal. There is marked increase of the lag as the signal increases above $10 ke^-$, and the peak image lag reaches 1.2% of the stored charge, consistent with previous measurements of similar PPD sensors.

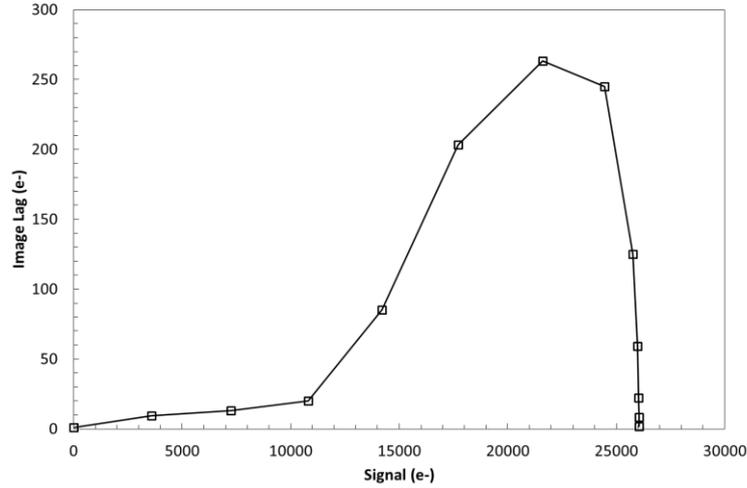


Figure 10. Image lag as a function of the stored charge in the PPD.

Global Shutter Efficiency

Ideally, devices with global shutter functionality should have no parasitic light sensitivity when the shutter is closed, corresponding to perfect shutter efficiency. Real world sensors, however, do have some parasitic light sensitivity, affecting the stored charge in pixel while the next image is being integrated.

CIS109 uses voltage domain signal storage on capacitors and is therefore expected to have very good global shutter efficiency. Any parasitic light sensitivity is expected to show up as charge or discharge of C1 and C2 by photogenerated currents in the p-n junctions connected to the capacitors, such as the source regions of M6 and M8.

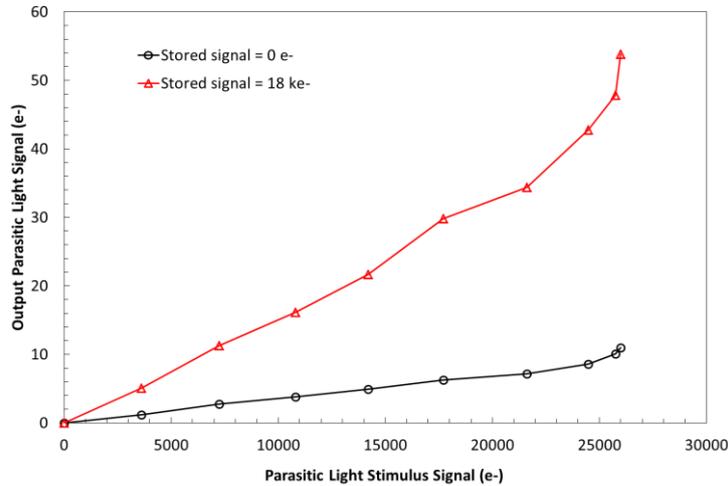


Figure 11. Parasitic light sensitivity in CIS109.

Figure 11 shows the measured parasitic signal due to light illumination in the cases when the stored signal is zero and near full well. The parasitic light stimulus was projected on the device in the time interval between the global image capture and the global pixel reset by RSTPD, followed by the readout as shown in Figure 2. During that time the main signal is stored as voltage on the capacitors C1 and C2. The parasitic light was generated by the same LED used to create the main charge. The duration of parasitic LED illumination was chosen from the photoresponse of the sensor in Figure 7 to generate a signal which would have been transferred out of the PPD in normal operation.

The parasitic light signal increases the sensor output at nearly full well by about $50 e^-$, or 0.2% of the parasitic signal, corresponding to 99.8% (54 dB) shutter efficiency. The parasitic light sensitivity at zero stored signal is a factor of 5 better, giving 99.96% shutter efficiency.

4. DISCUSSION

The proposed pixel architecture in this paper offers several advantages over previous designs. The use of PPD instead of 3T design⁵ helps reduce the capacitance of the floating diffusion and increases sensitivity. The bias current in the first stage source follower is gated by adding the switch M5, which greatly reduces power consumption, and global charge reset is accomplished by M1 (Figure 1). The fixed offsets of the CDS circuit can be removed by the column readout altogether, at the expense of a second row signal sample. The resulting sensor output is differential and this helps suppress common mode noise.

Compared to reported 8T and 9T designs⁷⁻⁹, this circuit does not use charge sharing between the reset and the signal samples, stored in the in-pixel capacitors. Due to the lack of capacitive division between the two samples the signal amplitude is not attenuated, and this increases the device sensitivity under identical conditions.

The readout noise of the sensor is approximately double that of an equivalent 4T sensor, using the same first stage source follower, CVF and column readout circuitry. While most of this noise increase can be attributed to the in-pixel signal storage, simulations show that there is a good agreement between the expected and the measured readout noise of CIS109.

Due to the two storage capacitors and the number of transistors per pixel the fill factor of the described sensor is 25%. The fill factor can be significantly improved if microlenses are used, or if the sensor is manufactured in backside illuminated variant, as the signal storage is in the voltage domain and no additional parasitic optical sensitivity is expected.

During the global image capture all first stage source followers in the imager are biased with the current I_{PIX} and this could make device scaling difficult, when applied to large imaging arrays. The instantaneous current consumption could be several hundred milliamps and may necessitate careful design of the supply metal tracks in order to minimize the resistive voltage drop. An alternative pixel design which eliminates the standing current of M7 may be possible and will be considered for the next, improved version of the device.

5. CONCLUSION

The presented image sensor is a promising pixel design for traditional global shutter applications such as high speed and hyperspectral imaging. The sensor's architecture offers several advantages over existing designs which improve the sensitivity and system integration. The device achieves low noise operation and has 71 dB dynamic range combined with good global shutter efficiency. The CIS109 was designed as a test bed for evaluation of global shutter pixel architectures and further developments will be necessary to manufacture a larger device capable of satisfying system requirements.

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